FIR FILTER
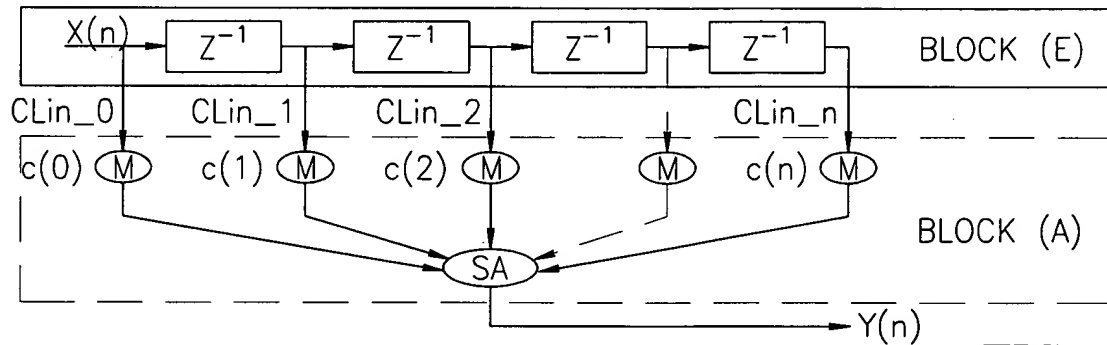

FIG. 1A

IIR FILTER
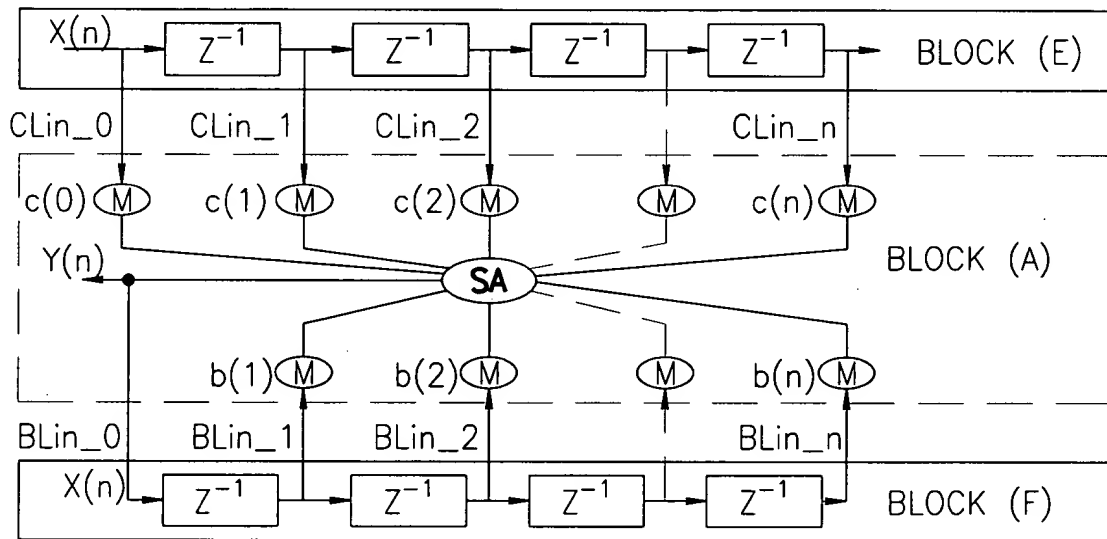

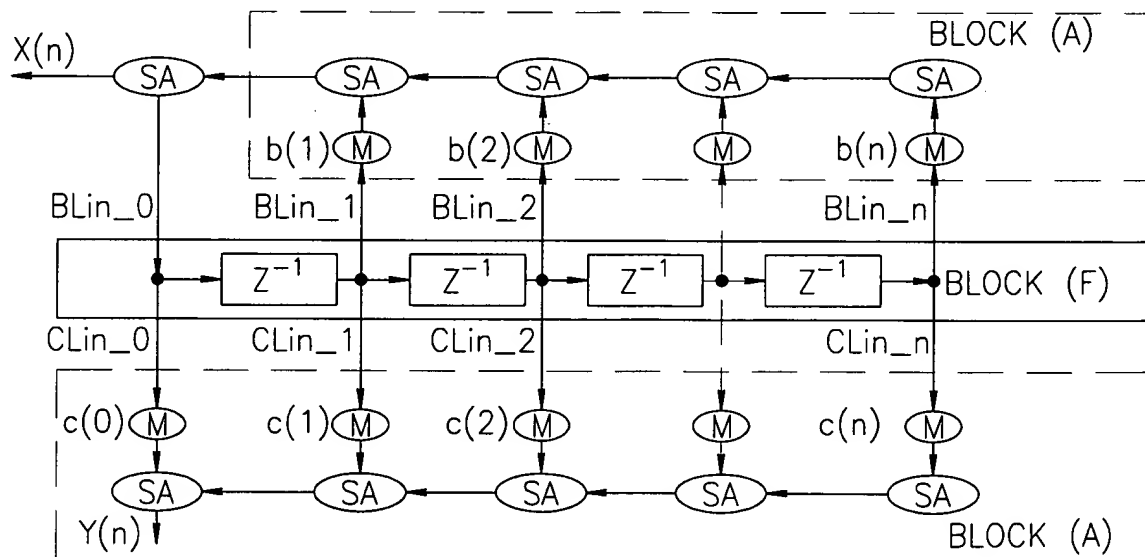FIG. 1B

FIG. 1C

BIT SERIAL ELEMENTS/COMPONENTS
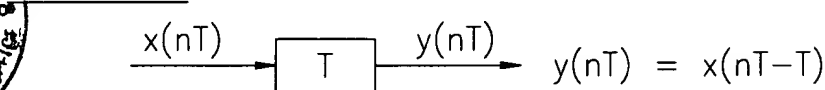
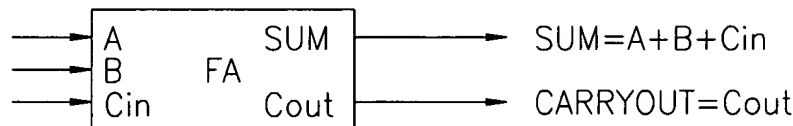UNIT DELAY

$$x(nT) \rightarrow \boxed{T} \rightarrow y(nT) \qquad y(nT) = x(nT-T)$$

FIG. 2A

FULL ADDER

A, B, Cin → [FA] → SUM, Cout

SUM=A+B+Cin

CARRYOUT=Cout

FIG. 2B

FULL SUBTRACTOR

A(+), B(−), Cin → [FA] → DIFF, Cout

DIFF=A−B−Cin

BORROW−OUT=Cout
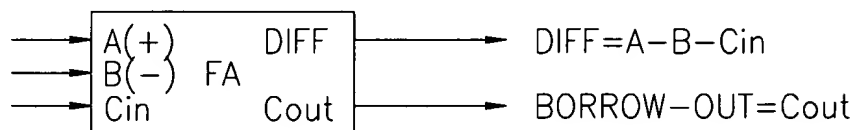
FIG. 2C

SERIAL ADDER

$x_1(nt)$, $x_2(nT)$ → (SA) → $y(nT)$
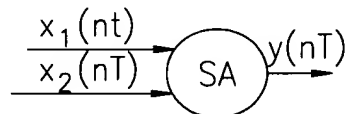
$y(nT)=x_1(nT)+x_2(nT)$ *FIG. 2D*

SERIAL SUBTRACTOR

$x_1(nt)$, $x_2(nT)$ → (SS (−)) → $y(nT)$
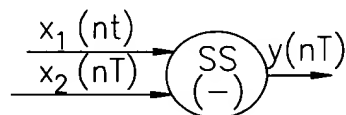
$y(nT)=x_1(nT)-x_2(nT)$ *FIG. 2E*

MULTIPLIER

m

$x(nT)$ → (M) → $y(nT)$
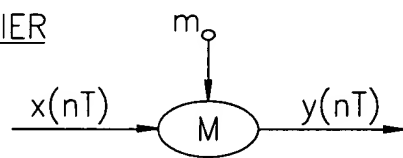
$y(nT)=m*x(nT)$ *FIG. 2F*

DELAY

INPUT FRAME SIZE = X BITS (E.G INPUT IS 1010101 OR X=7 BITS)

TO STORE X BIT FRAME, NUMBER OF T ELEMENT
USED IN X OR 7 IN PRESENT CASE

SERIAL ONE BIT INPUT
FRAME SIZE (X BITS)   SERIAL ONE BIT OUTPUT
                             FRAME SIZE (X BITS)

$$\boxed{Z^{-1}}$$

SERIAL ONE BIT INPUT   OR
FRAME SIZE (X BITS) | T | T | T | T | | T | T | T |

Eq $y(n)=x(n-1)$

FIG. 2G

UNIT DELAY

x(nT) $\xrightarrow{(0101011)}$ [D Q^T CLK] $\xrightarrow{(01010110)}$ OUTPUT

FIG. 3A

INPUT FRAME INPUT PATTERN (0101011) IS COMING SERIALLY
AT x(nt) PIN AT CLOCK RATE SPECIFIED ON CLOCK PIN
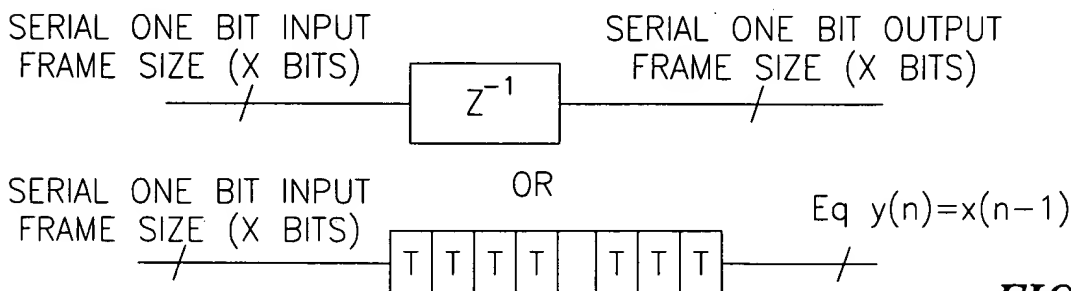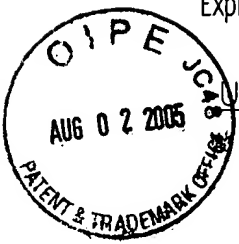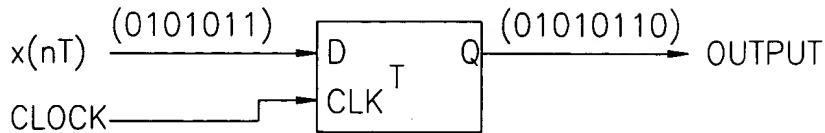
FULL ADDER (FA) / FULL SUBTRACTOR (FS)

BINARY ADDITION/SUBTRACTION COMPONENTS IS REALIZED
USING FOLLOWING TRUTH TABLE

| TRUTH TABLE—FULL ADDER | | | | | | TRUTH TABLE—FULL SUBTRACTOR | | | | |
A	B	Cin	Z	Co		A	B	Cin	Z	Co
0	0	0	0	0		0	0	0	0	0
0	0	1	1	0		0	0	1	1	1
0	1	0	1	0		0	1	0	1	1
0	1	1	0	1		0	1	1	0	1
1	0	0	1	0		1	0	0	1	0
1	0	1	0	1		1	0	1	0	0
1	1	0	0	1		1	1	0	0	0
1	1	1	1	1		1	1	1	1	1

FIG. 3B

SERIAL ADDER (SA) / SUBTRACTOR (SS)
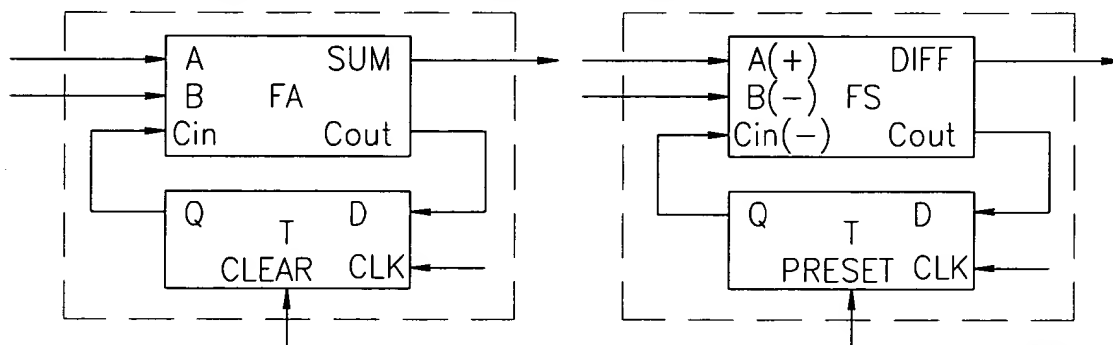
FIG. 3C

SERIAL MULTIPLIER(M)   m=331(INTEGER)
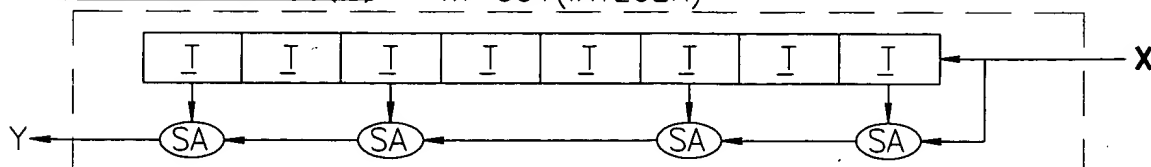
BIT MULTIPLIER COEFFICIENT SIZE IN THIS
EXAMPLE IS 331 (BINARY 101001011)

FIG. 3D

IMPLEMENTATION 1

INPUT

CLin_n   CLin_2   CLin_1   CLin_0

BLOCK(A)   COEFFICIENT
                            BLOCK

c(n) (M) ...... (M)   (M) c(2)   c(1) (M)   c(0) (M)

CLout_n   CLout_2   CLout_1   CLout_0

BLOCK(E) Z^{-1} (SA) Z^{-1} (SA) Z^{-1} (SA) Z^{-1} (SA)
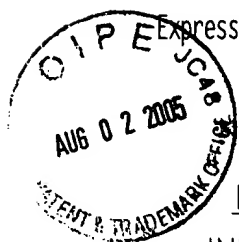
REALIZATION OF COEFFICIENT USING SHARE–ABLE
MULTIPLIER (COEFF.=3.11)

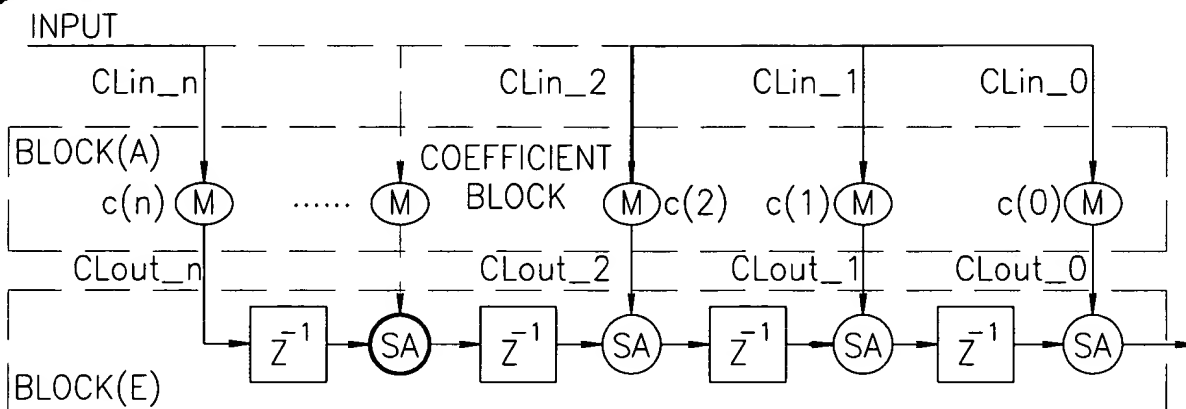INPUT —— | T | T | T |

(SA)   (SA)

INPUT*3   INPUT*11   *FIG. 4A*

IMPLEMENTATION 2

BLOCK (E)
INPUT — Z^{-1} — Z^{-1} — Z^{-1} — Z^{-1} — — — Z^{-1}

CLin_0   CLin_1   CLin_2   CLin_n

c(0) (M) c(1) (M) c(2) (M) c(3) (M) .... (M)   c(n) (M)

(SA)   (SA)   (SA)   (SA)   (SA)

BLOCK (A)   COEFFICENT BLOCK

FIG. 4B

INPUT

CLin_0   CLin_1   CLin_2   CLin_3   CLin_4   CLin_5   CLin_6

Z^{-1} Z^{-1} Z^{-1} Z^{-1} Z^{-1} Z^{-1}

M^5 M^{14} M^{25} M^{30} M^{25} M^{14} M^5

SA   SA   SA   SA   SA   SA

BLOCK (A)   OUTPUT

FIG. 5
PRIOR ART

INPUT

Z^{-1} Z^{-1} Z^{-1} Z^{-1} Z^{-1} Z^{-1}

CLin_0   CLin_1   CLin_2   CLin_3   CLin_4   CLin_5   CLin_6

SA(1)   SA(2)   SA(3)

S1   S2   S3   S4

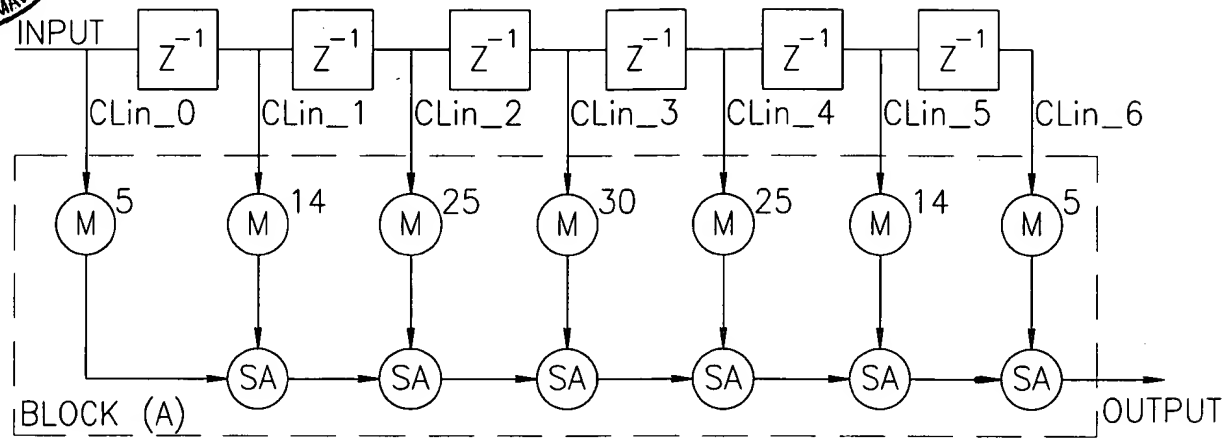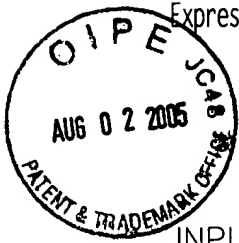5 M(1)   14 M(2)   25 M(3)   30 M(4)

SA(4)   SA(5)   SA(6)   OUTPUT

BLOCK (A)
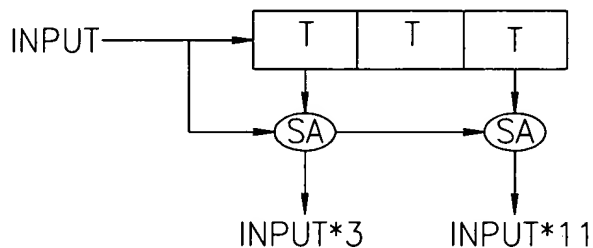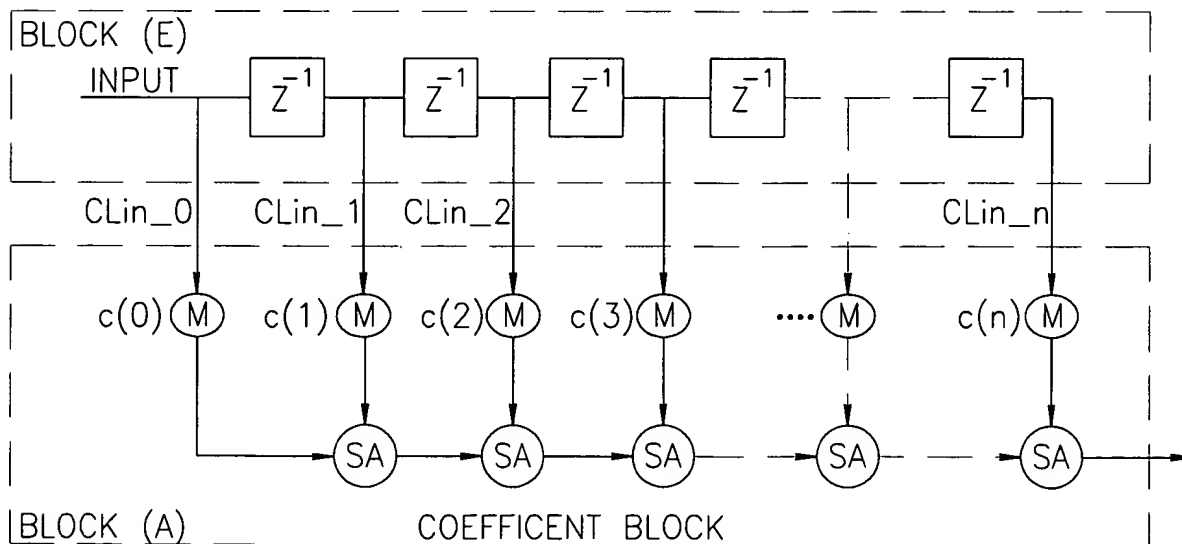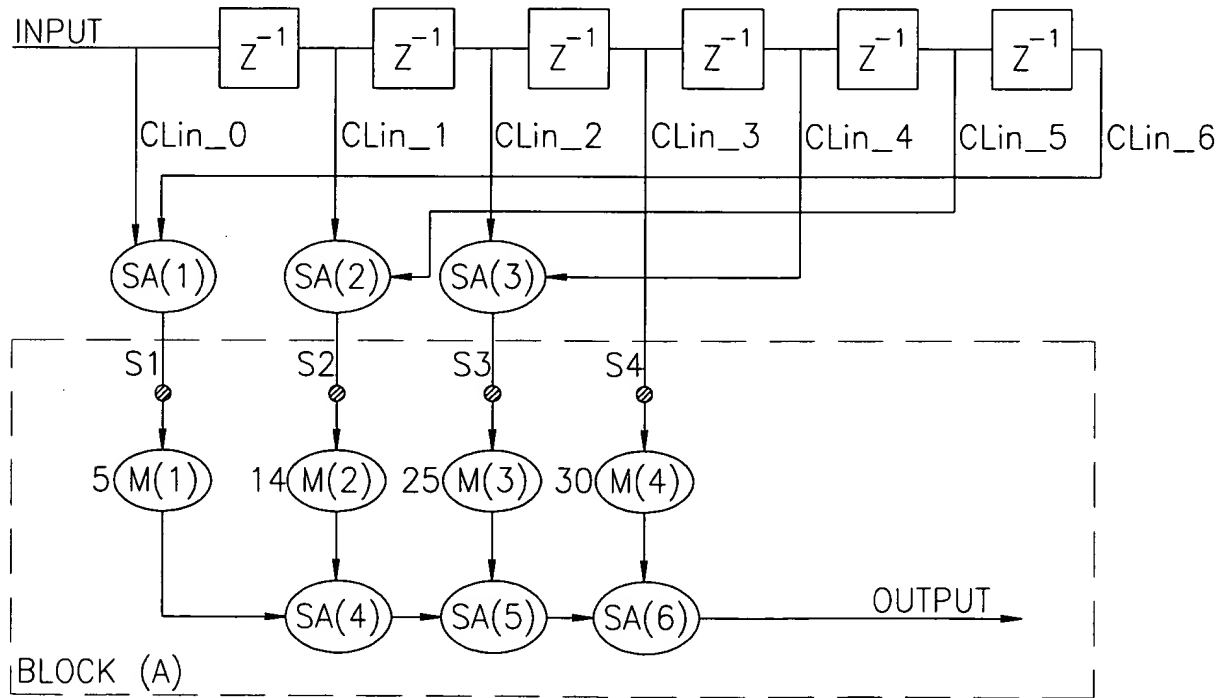
FIG. 6
PRIOR ART

FIG. 7
PRIOR ART

A) APPROX. NUMBER OF SA = NUMBER OF COEFFICIENT * (MAX COEFF SIZE /2)
B) FLIP-FLOP (T) ARE NOT SHARABLE
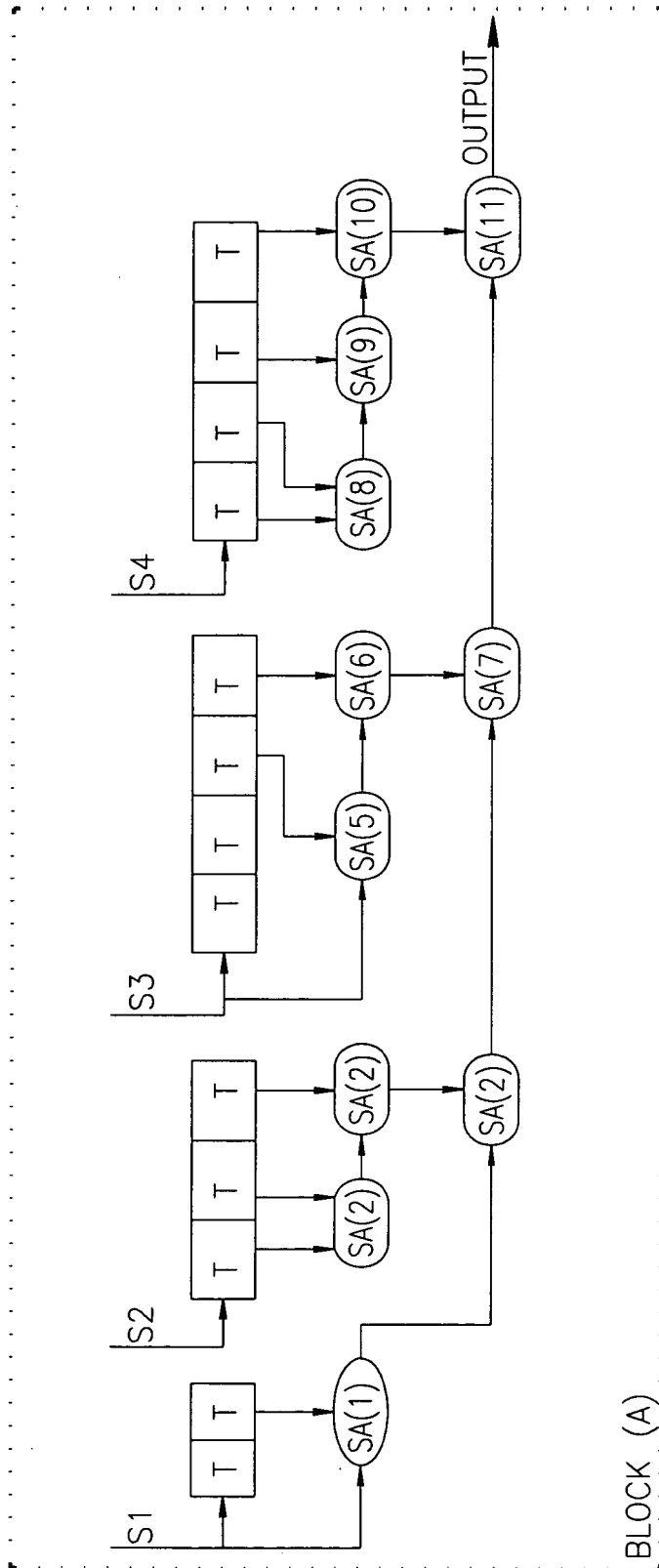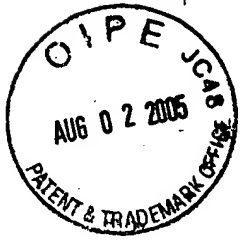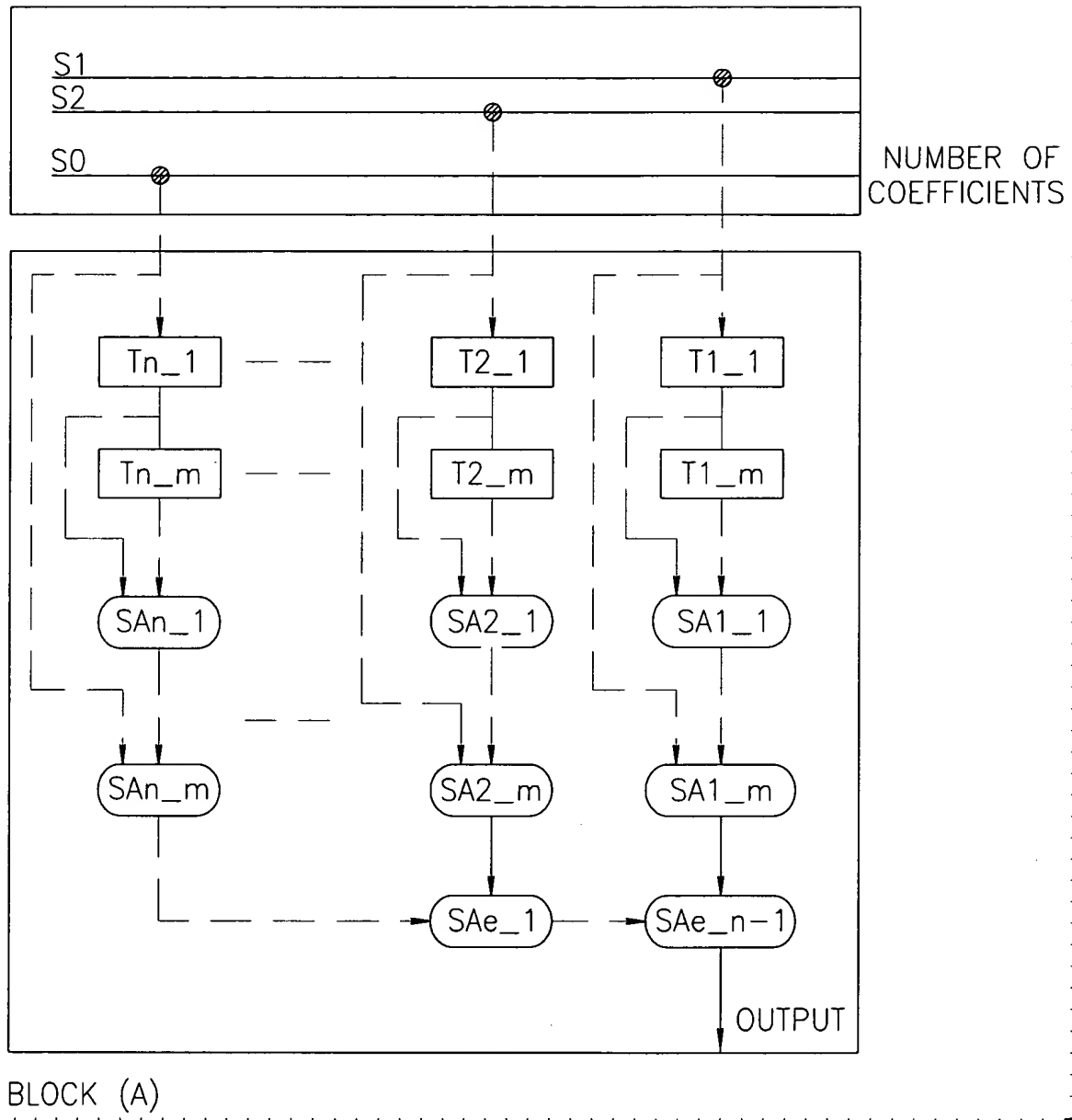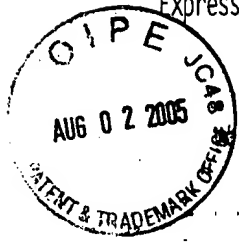   APPROX. NUMBER OF FLIP-FLOPS – NUMBER OF COEFF * (MAX. COEFFICIENT SIZE /2)

FIG. 8
PRIOR ART

FIG. 9

BIT POSITIONS

2^m 2^1 2^0

BLOCK(A)   BITm   BIT1   BIT0

S1   S1–Sn=NUMBER OF COEFFICIENTS

S2

Sn

BLOCK(D)   COMBINATIONAL
–SEQUENTIAL
BLOCK(D)

SAm_1   SAm–1_1   SAm_1   SA0_1

BLOCK(B)   BLOCK(B)   BLOCK(B)   BLOCK(B)

$(am*S1+bm*S2+.....+km*sr$

$(am*S1+b1*S2+.....+k1*sn)$

$(a0*S1+b0*S2+.....+k0*sn)$

SAm_n   SAm–1_n   SA1_n   SA0_n   TERMS REPRESENTING ADDITION

b_m   b_2   b_1

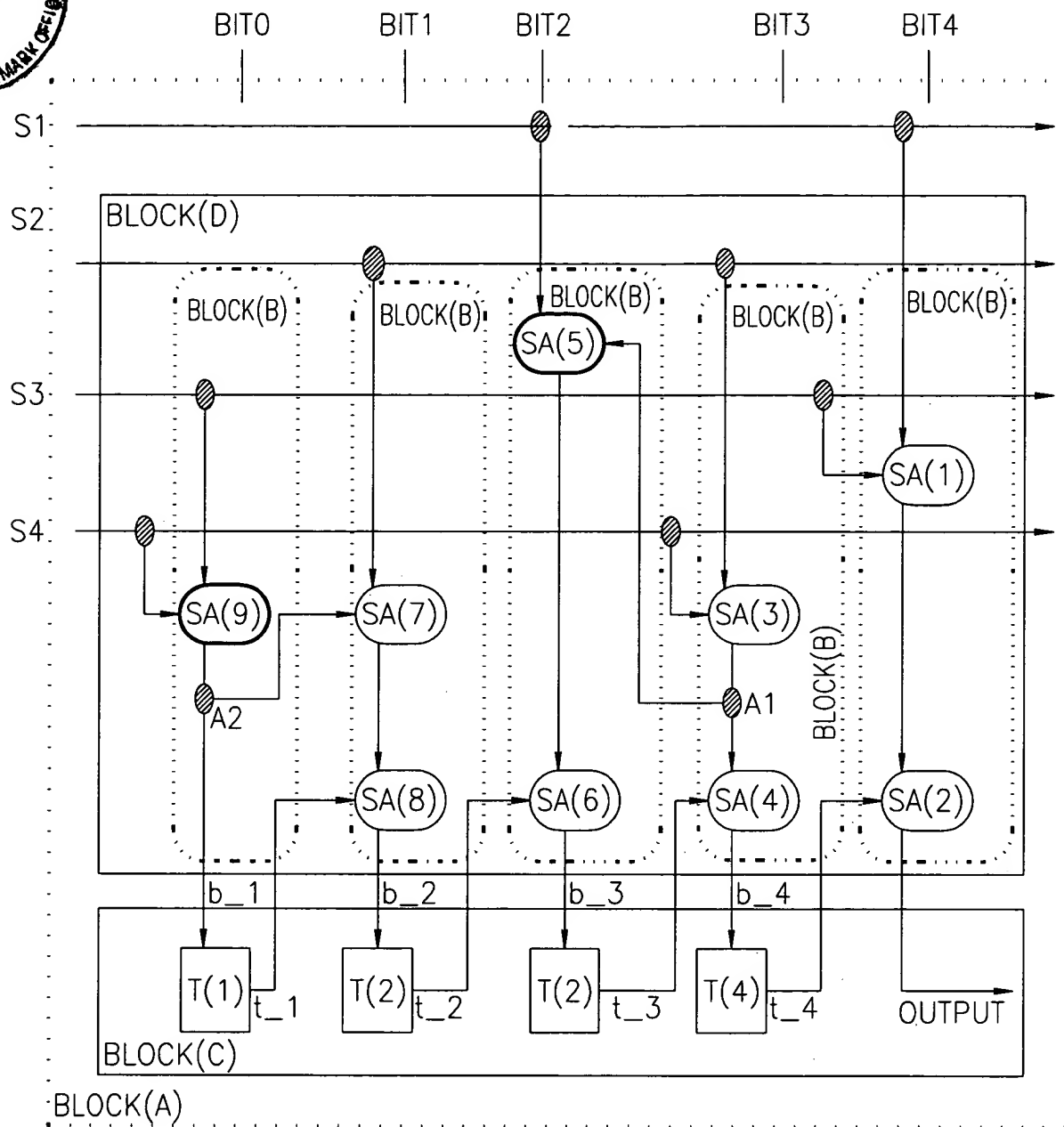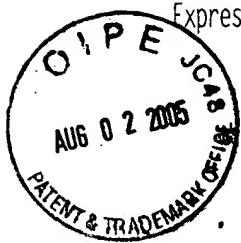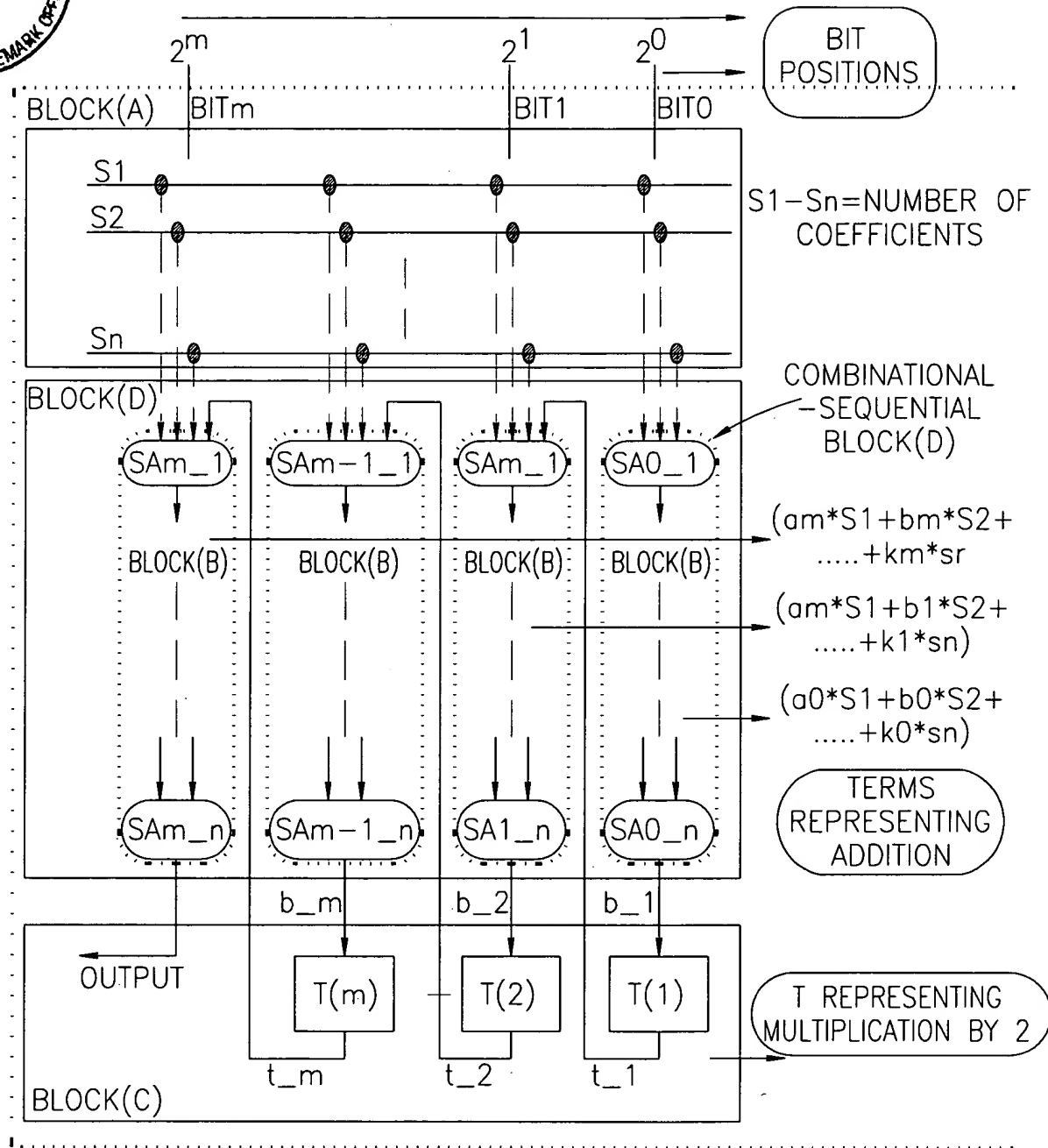OUTPUT   T(m)   T(2)   T(1)   T REPRESENTING MULTIPLICATION BY 2

t_m   t_2   t_1

BLOCK(C)

APPROX. NUMBER OF SERIAL ADDERS = (NUMBER OF COEFFICIENT MAX COEFF SIZE /2)
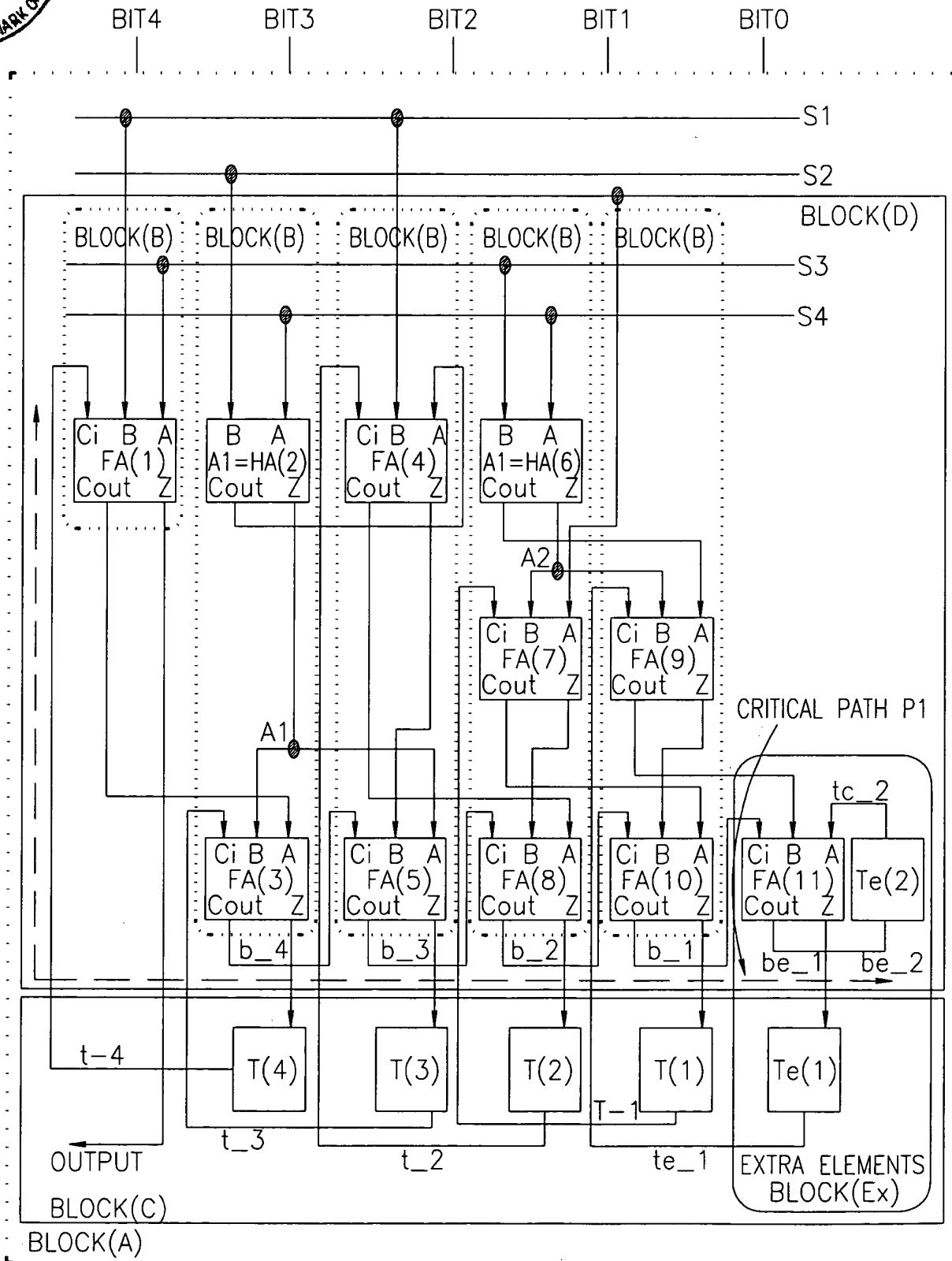NUMBER OF FLIP – FLOPS(I) = SIZE OF MAXIMUM COEFFICIENT

FIG. 10

FIG. 11
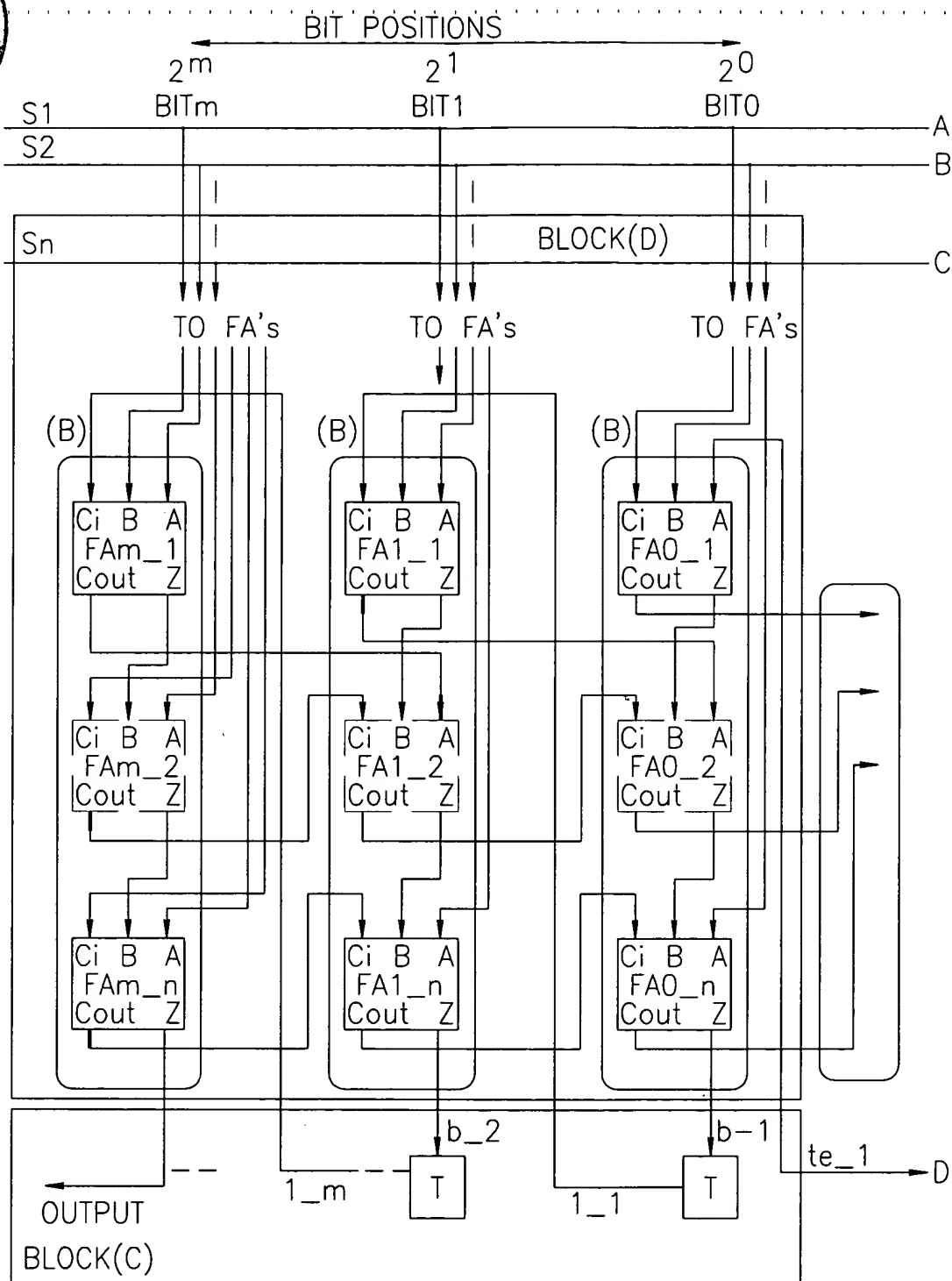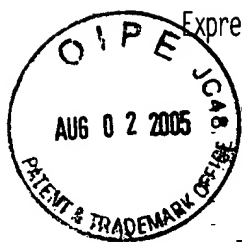
NUMBER OF FLIP-FLOPS = MAXIMUM SIZE OF COEFFICIENT
NUMBER OD ADDERS = <NUM. OF COEFF MAXIMUM COEFF. SIXE /2

FIG. 12A

A

B

C

TO
EXTRA
ELEMENTS

Ci B A
FAO_1e
Cout Z

Te(1)

Ci B A
FAO_2e
Cout Z

Te(2)

Ci B A
FAO_4e
Cout Z

Te(4)

Ci B A
FAO_5e
Cout Z

Te(5)

Ci B A
FAO_3e
Cout Z

Te(3)

Ci B A
FAO_6e
Cout Z

Te(6)

CARRY−OUT
OF PREVIOUS
SECTION NUMBER
OF ADDERS
OF PREVIOUS
STAGE

Ci B A
FAO_7e
Cout Z

Te(7)

D ─ Te

BLOCK(Ex)
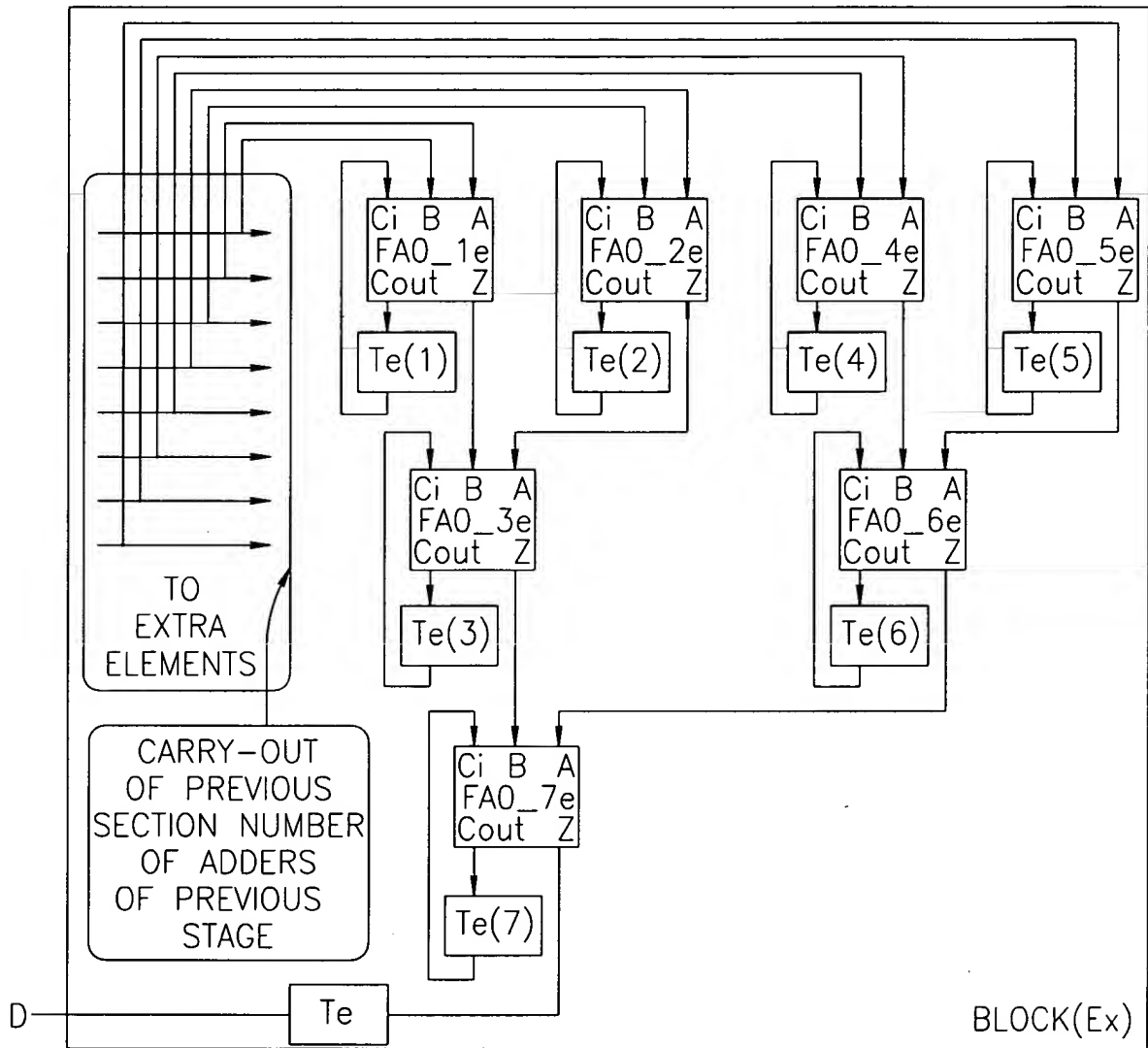
EXTRA ELEMENTS
NUMBER OF T− ELEMENTS = NUMBER OF ADDERS OF LAST STAGE
NUMBER OD FA− ELEMENTS = NUMBER OF ADDERS OF LAST STAGE−1
AN EXAMPLE II NUMB. OF ADDERS IN PREVIOUS STAGE − B,
NUMBER OF T−ELEMENTS, FA−ELEMENTS = 8, 7 RESPECTIVELY.

BLOCK(A)

FIG. 12B

BIT3   BIT2   BIT1   BIT0

BLOCK(A)

S1
S2
S3
S4

BLOCK(B)   BLOCK(B)   BLOCK(B)   BLOCK(B)   BLOCK(B)

Ci B A   B A   Ci B A   B A
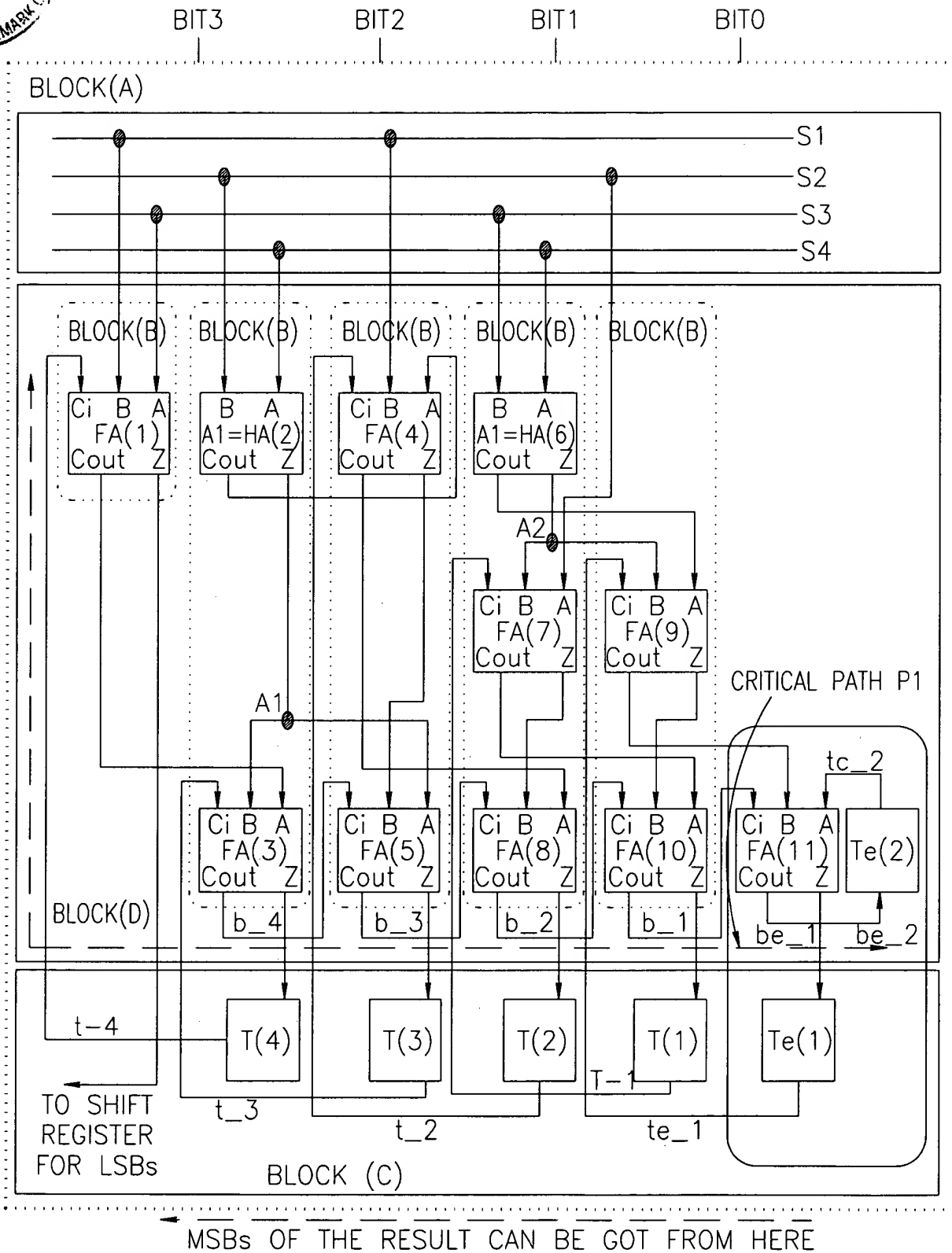FA(1)   A1=HA(2)   FA(4)   A1=HA(6)
Cout Z   Cout Z   Cout Z   Cout Z

A2

Ci B A   Ci B A
FA(7)   FA(9)
Cout Z   Cout Z

CRITICAL PATH P1

A1

tc_2

Ci B A   Ci B A   Ci B A   Ci B A   Ci B A
FA(3)   FA(5)   FA(8)   FA(10)   FA(11)   Te(2)
Cout Z   Cout Z   Cout Z   Cout Z   Cout Z

BLOCK(D)
b_4   b_3   b_2   b_1   be_1   be_2

t-4
T(4)   T(3)   T(2)   T(1)   Te(1)

TO SHIFT   t_3
REGISTER   t_2   te_1
FOR LSBs   BLOCK (C)   T-1

← MSBs OF THE RESULT CAN BE GOT FROM HERE

FIG. 13